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Patentanmeldung Nr. Patent application No. Demande de brevet n°

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LUCENT TECHNOLOGIES INC.
Murray Hill, New Jersey 07974-0636
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Accumulative ARQ method and system

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The original title of the application reads as follows : Diversity selective automatic repeat request

DIVERSITY SELECTIVE AUTOMATIC REPEAT REQUEST

Field of the Invention

This invention relates to communication systems that utilise packet retransmission schemes to correct errors, and particularly but not
5 exclusively to mobile telecommunications systems utilising such schemes.

Background to the Invention

Digital mobile communication using radio waves suffer from errors due to fading and unwanted interference. Even in communication systems where the transmission channel is not radio based errors occur due to presence of
10 noise in most of the human made devices. To correct these errors two main techniques are used nowadays in the telecommunication industry, namely forward error correcting coding and packet retransmission techniques. The latter method is mostly used in packet switched networks where a very low bit error rate is required and the packet delay constraint is not too tight.

15 The most efficient packet retransmission protocol is based on a selective automatic repeat request (ARQ) scheme. In this scheme the transmitter sends several data packets over an interface (e.g. radio channel) to the receiver. The data packets are protected by, for example, a cyclic redundancy check (CRC) code, which is used by the receiver to detect errors
20 within a received data packet. If errors are detected by the CRC check then the receiver sends a negative acknowledgement signal to the transmitter to inform it of the erroneous packets. On the receipt of a negative acknowledgement signal, the transmitter retransmits only those data packets indicated by the negative acknowledgement signal as being in error.

25 This retransmission process is repeated until either the CRC check is passed by all transmitted data packets or until the maximum allowed number of retransmissions is reached, or the delay per packet expires. Examples of this basic selective ARQ scheme may be found in the following papers: "Energy-conserving selective repeat ARQ protocols for wireless data networks", I.
30 Chlamtac et al., Proc. PIRME, 1998; "Optimal design of error control

schemes for packet radio networks", S. Gupta and M. E. Zarki, Proc. of International Conference on Personal Wireless Communications, 1994, pp. 229-233; and "Throughput analysis of ARQ selective-repeat protocol with time diversity in Markov channels", Proc. IEEE Globecom, 1995, pp. 1673-1677.

- In this basic selective ARQ scheme, if a data packet fails the CRC check then this packet is discarded and its retransmission requested. This approach leads to poor throughput and large packet transmission delay especially for systems having a low signal-to-noise ratio (SNR).
- 10 In an alternative scheme, the erroneously received data packets are not discarded at the receiver but used to improve the data packet reliability by combining them with the next retransmitted copy of the same packet. This packet combining approach has been disclosed in several papers, for example: "Code Combining-a maximum likelihood decoding approach for
- 15 combining an arbitrary number of noisy packets", D. Chase, IEEE Transactions on Communications, vol. COM-33, No. 5, 1985, pp. 385-393; "Type-1 hybrid ARQ scheme with time diversity for binary digital FM cellular radio", H. Zhou and R. H. Deng, IEE Proceedings on Communications, vol. 143, No. 1, 1996, pp. 29-36; and "Performance of
- 20 punctured channel codes with ARQ for multimedia transmission in Rayleigh fading channels", H. Lou and A. S. Cheung, IEEE Vehicular Technologies Conference 46th, 1996, pp. 282-286.

However the packet combining techniques used in these papers minimise the packet error probability rather than the bit error probability.

- 25 In "Performance of punctured channel codes with ARQ for multimedia transmission in Rayleigh fading channels", H. Lou and A. S. Cheung, IEEE Vehicular Technologies Conference 46th, 1996, pp. 282-286 the authors present a type-II hybrid ARQ scheme (incremental redundancy) where more parity bits are sent whenever the CRC check on a data packet fails.

It is therefore an object of the present invention to provide an improved repeat transmission combining scheme.

Summary of the Invention

5 This invention relates to an error correction method for data packets based on the automatic repeat packet retransmission mechanism. In particular a symbol-by-symbol optimal combining of the erroneous received data packets is presented.

According to the invention there is provided a method of recovering a received packet comprising the steps of:

- 10 a) generating a soft value for each bit of the received packet;
- b) storing the soft values of the received packet;
- c) performing an error check on the received packet; and
- d) responsive to detection of an error:
 - i) receiving a retransmission of the packet;
 - 15 ii) generating a soft value for each bit of the retransmitted packet;
 - iii) combining each generated soft value with the respective last stored soft values;
 - iv) storing the combined soft values;
 - v) performing an error check based on the thus combined soft values;
 - 20 and
 - vi) responsive to detection of an error repeating steps i) to v).

The step of combining each soft output value of the retransmitted packet with the respective stored soft output value may comprise adding the respective soft values.

- 25 The method may comprise the step of determining a hard value from the soft values of the received packet. The error check of step c) may be performed on said hard value.

The method may further comprise the step of determining a hard value from the combined soft values. The error check of step v) may be performed on said hard value.

5 The method may further comprise the step, prior to the step a) or i), of equalising the received packet. The error check may comprise a cyclic redundancy code check. In step vi), steps i) to v) may be repeated a predetermined number of times. In step vi), steps i) to v) may be repeated for the maximum number of retransmissions allowed by the system, or for the maximum delay per packet.

10 The invention also provides receiver circuitry for implementing such a method.

According to a further aspect of the invention there is also provided a receiver comprising:

- e) input circuitry for receiving a transmitted packet;
- 15 f) generating circuitry, connected to the input circuitry, for generating a soft value for each bit of the received packet;
- g) storage circuitry for storing the thus generated soft values;
- h) error checking circuitry for performing an error check on the received packet; and
- 20 i) combining circuitry, wherein responsive to detection of an error:
 - i) the input circuitry receives a retransmission of the packet;
 - ii) the generating circuitry generates a soft value for each bit of the retransmitted packet;
 - iii) the combining circuitry combines each generated soft value with
 - 25 the respective stored soft values;
 - iv) the storage circuitry stores combined soft values in place of the stored soft values;

- v) the error checking circuitry performs an error check based on the thus combined soft values,
- vi) wherein i) to v) are repeated responsive to detection of an error in v).

5 A mobile communications system may include such a receiver.

This invention is concerned with a type 1 hybrid selective ARQ mechanism where both the information bits and the parity bits are retransmitted when a negative acknowledgement is received by the transmitter. This invention introduces a novel and optimal symbol-by-symbol soft combining technique.

10 The ARQ scheme proposed in this invention is less complex than those combining techniques proposed in the references discussed above, and therefore easier to implement on a real telecommunication system.

Brief Description of the Drawings

Figure 1 illustrates a flow chart of an exemplary implementation of the present invention;

Figure 2 illustrates an exemplary implementation of the present invention;

Figures 3(a) to 3(c) illustrate performance characteristics of the present invention compared to prior art techniques; and

Figure 4 illustrates exemplary performance characteristics of the present invention.

Description of the Preferred Embodiment

The soft combining technique according to the invention will now be described with reference to Figures 1 and 2. Figure 1 is a flow chart of an exemplary implementation of the invention, and Figure 2 is an exemplary implementation of circuitry for implementing the steps illustrated in Figure 1.

Referring to Figure 2 it can be seen that the receiver circuitry includes input/output circuitry 100, soft-output equaliser circuitry 102, a decoder

106, error checking circuitry 108, a buffer 110, a combiner 112, and a control circuit 114.

The receiver circuitry is connected to a transmission line 116 which is the transmission interface between the receiver and a transmitter (not shown).

5 The input/output circuitry 100 is connected to the transmission line 116, and outputs received data packets on line 118 to the soft-output equaliser circuitry 102. The soft-output equaliser circuitry 102 outputs signals on line 122 to the decoder 106, the buffer 110 and the combiner 112. The decoder outputs signals on line 126 to the error checking circuitry 108. The error
10 checking circuitry 108 outputs a signal on line 128 to the control circuit 114. The buffer outputs a signal on line 130 to the combiner 112, and the combiner outputs a signal on line 132 to the buffer 110 and the decoder 106. Each of the input/output circuitry 100, soft-output equaliser circuitry 102, decoder 106, error checking circuitry 108, buffer 110, and combiner 112
15 receive control signals from the control circuit 114. The signal on line 126 from the decoder 106 is presented to other parts of the receiver circuitry (not shown) for further processing after the error correction as described below

This invention can be implemented for the general packet radio services (GPRS) for GSM (see "Digital cellular telecommunications system; General
20 radio service (GPRS); Mobile station-Base station subsystem Radio Control Layer/Medium access control layer specification, GSM 04.60). However this invention is not restricted to GSM systems and can be implemented in any communication system which includes a soft-output equaliser and an error-detecting device, and where packets are sent from a transmitter to a
25 receiver and which has a repeat request mechanism. For the purposes of illustrating the present invention in the following description a specific example of a receiver in relation to a GPRS system is given, but it will be appreciated that the invention may be implemented in alternative receivers. The following example specifically relates to a GPRS system. RLC/MAC
30 blocks are the smallest packet within GPRS.

In a first step 2 the input/output circuitry receives an Mth radio link control (RLC)/ medium access control (MAC) block, including an nth transmitted packet, on the communications link 116 from the transmitter (not shown). In this example the block is transmitted over a radio interface, but it will be appreciated that the invention may be utilised on any type of interface, wireless or otherwise.

The format of the particular block and the packets contained therein is not important to the present invention, and the present invention can be implemented with any type of blocks or packets.

10 In a step 4 the soft-output equaliser circuitry 102 inputs the received block including the nth data packet from the input/output circuitry on line 118, and performs channel estimation and then channel equalisation, the implementation of which will be familiar to one skilled in the art.

15 If the transmitter (i.e. the mobile station or the base transceiver station) is multi-time slot capable then the equaliser shown in Figure 1 is formed by many equalisers; one for each timeslot used by the transmitter, and there is also one buffer associated with each equaliser. These buffers communicate to one another either by sharing the same physical memory or by other mechanism which is outside the scope of the present invention. Thus when a
20 time-slot used for a radio channel is changed during a transmission then the buffer content corresponding to the previous time-slot is stored into the buffer corresponding to the newly allocated radio channel. Thus, the system operates even when the radio channel is reassigned. The reference to time-slots does not restrict the implementation of this algorithm. Any
25 transmission channel has a buffer allocated and all buffers communicate to one another.

In a step 6 the soft output equaliser circuitry 102 generates the soft output for each data packet in the received block, and outputs these soft outputs on lines 122. The thus generated soft outputs are presented on signal lines 122
30 to the decoder 106 and the buffer 110.

The soft output of each bit of a packet is SO, where:

$$SO = \log \frac{\{\text{probability that bit} = 1, \text{ conditioned by received signal}\}}{\{\text{probability that bit} = 0, \text{ conditioned by received signal}\}}$$

Thus, the soft output is basically the logarithm of a ratio of two probabilities. This generation of soft values is known. If the result of this calculation is positive it is estimated that the bit is 1, otherwise the bit is 0.

Not shown in Figure 1, but understood by one skilled in the art, is the step of de-interleaving the received block to recover the transmitted packets included in the block in their original order. This de-interleaving may be done at the output of the soft output equaliser circuitry 102.

It will be appreciated that the operation of the receiver circuitry described herein is controlled by the control circuit 114. The specific control of the various blocks in the receiver circuitry is outside the scope of the invention and is not presented here in detail. Only those aspects of the operation of the control circuit considered necessary to describe the invention are described.

Under control of the control signals 124 from the control circuit 114 the soft outputs of the received block on line 122 are stored in the buffer 110 in a step 8. At the same time the soft outputs on lines 122 are decoded by the decoder 106 in a step 10 to produce a hard output for each packet of the received block. The hard outputs are then presented on lines 126 to the error check circuit 108. The decoder decodes the soft output values, i.e. determines whether the result of the logarithm for each bit is 1 or 0 and outputs the appropriate bit, this being the hard value.

In a step 12 the error checking circuitry performs an error check on the decoded hard output packets of the received block, and generates a signal on line 128 to the control circuit 114 indicating the result of the error check for each packet of the block. In the preferred embodiment the error check is a CRC check, performed over each individual packet such that the error check generates an error signal for each individual packet. If the error signal on

line 114 indicates, in a step 14, that no errors are detected for all packets of the block, then the control circuit controls other circuitry in the receiver via control lines 124 to receive the hard value at the output of the decoder on lines 126. The hard value is then presented on line 126 to circuitry
5 elsewhere in the receiving circuitry for further decoding and routing. This is represented by step 16.

If no errors are detected, then in a step 42 the control circuit 114 controls the input/output circuitry 100 via lines 124 to send an acknowledgement signal back to the transmitter. This acknowledgement signal indicates the
10 successful transmission of an RLC/MAC block. The transmitter then sends the next block and the input/output circuitry 100 receives the next block on the transmission line 116. Steps 2 to 12 are repeated for that block.

If the error signal on line 128 from the error check circuit 108 indicates, in step 14, that the decoded hard output of at least one data packet of the
15 block, say the nth data packet, has failed the error check, then the control circuit controls the input/output circuitry via lines 124 to request the transmitter, via lines 116, to retransmit that same data packet again. The input/output circuitry 100 thus sends a negative acknowledgement signal to the transmitter on lines 116, as illustrated by step 18. The negative
20 acknowledgement signal identifies the failed data packet.

Responsive to the negative acknowledgement signal, the transmitter (not shown) retransmits the nth data packet again, and as illustrated by step 20 the input/output circuitry 100 once again receives the nth data packet on the transmission line 116.

25 It will be appreciated that several packets in one block may fail the error check, and consequently several packets be retransmitted. The buffer will store the original of those packets and then the combination result of those packets as described below. Packets will pass the error checks after different numbers of retransmissions.

The frequency of sending the acknowledgement/negative acknowledgement signal is a trade off between the amount of memory required at the receiver to store all erroneously received RLC/MAC blocks and the reverse channel signalling overhead. In the same time the content of the buffer 110 which
5 stores the soft values of the error free RLC/MAC block is emptied when an acknowledgement for all stored soft value RLC/MAC blocks is sent back to the transmitter.

As before, the retransmitted nth data packet is output on line 118 to the soft-output equaliser circuitry 102 where it is equalised in a step 22. In a
10 step 24 the soft output equaliser circuitry 102 generates the soft values of the retransmitted data packet as before. The soft values of the retransmitted data packet are output on lines 122.

Under the control of the control lines 124 of the control circuit 114, the soft values on line 122 are presented to the combiner 112 together with the soft
15 values for the originally transmitted packet stored in the buffer 110. The soft values of the originally transmitted signal are presented on line 130 to the combiner 112.

In a step 26 the combiner 112 adds respective ones of the soft values associated with the retransmitted packet to respective ones of the soft
20 values stored in the buffer 110, which at this stage represent the soft output of the originally transmitted packet. The result of this combining operation is output on line 132, and stored in the buffer in place of the soft output of the originally transmitted signal. The buffer 110 thus stores the thus combined soft values.

25 According to the invention, the combiner 112 combines the soft values and not the hard values. This is the optimum combining technique because it minimises the bit error rate. By adding two soft values, i.e. the values SO, the probabilities at the argument of the log function are multiplied. As the packet retransmission processes are independent it can be proven
30 mathematically that the sum of all the SO values per bit (or product of

probabilities) gives the minimum bit error rate. This is a per bit optimisation: the combining scheme of the soft bit values (SO) which minimises the bit error rate. The outcome of this optimisation problem is that the sum of the soft values gives the minimum bit error rate. This is
5 very appealing from an implementation point of view, because the previous soft values can be simply added to the new soft values to give the optimum scheme.

This contrasts with the packet combining of the basic ARQ scheme described in the introduction. For packet combining a joint (global)
10 equalisation and decoding is performed packet by packet. A joint packet combining technique is found which minimises the packet error rate. In a multi-path environment when the equaliser is required this joint optimisation problem is very difficult to implement on a real system.

On the contrary, the present invention uses a simple bit by bit equaliser
15 which decouples the equalisation and decoding problems.

The drawback of packet combining is that the formulae produced by this joint optimisation problem are cumbersome and not easy to implement, whilst for bit combining a simple addition is all that is required.

The combined signal on lines 132 is also presented as an input to the
20 decoder 106. In a step 30 the decoder 106 decodes the combined soft values and presents the hard values on line 126 to the error check circuit 108. As before, in a step 32 the error check circuit performs an error check on the hard values and outputs a signal on line 128 to the control circuit 114 indicating the result of the error check.

25 In a step 34 the control circuit 114 determines whether the error check has passed or failed. If there is no error, then the control circuit 114, in a step 36, outputs the hard values on line 126 for processing in the receiver. In the step 42 the control circuit then controls the input/output circuitry 100 to send an acknowledgement signal to the transmitter, and prepares to receive

the next block M. the hard values on line 126 are derived directly from the combined soft values in the buffer 110.

If in the step 34 the error signals from the error check circuit still indicate that the error check has failed then the control circuit moves onto a step 38.

- 5 In the step 38 the control circuit determines whether it is appropriate to request a further retransmission of the data packet. If it is appropriate, then the steps 18 to 34 are repeated again and a further negative acknowledgement signal is sent to the transmitter, requesting a retransmission of the erroneous packet of the RLC/MAC block. On the
- 10 receipt of the retransmitted packet the receiver again derives the soft equalizer output for this packet as described above. This soft value is then added to the buffer content and their sum passed to the decoder. Mathematically this can be expressed as

$$L_k = \sum_{i=1}^{A_k} L_{ki}$$

- 15 where L_k is the total soft value corresponding to the k th received coded bit of a packet after N packet retransmissions. Similarly L_{ki} is the soft value corresponding to the k th received coded bit of a packet at the i th block retransmission. This bit-by-bit soft combining technique is optimal in minimising the bit error rate.
- 20 A packet of an RLC/MAC block is retransmitted a number of times until it passes the CRC check. The number of blocks combined gives the order of the diversity gain obtained in the proposed scheme. Thus this scheme may be called "Diversity-ARQ", to highlight the diversity gain and discriminate among others existing ARQ mechanisms.
- 25 If it is not appropriate to request further retransmissions, then the control circuit moves onto a step 40 in which the combined packet in the buffer 110 is output on line 130, together with an appropriate error signal for processing in the receiver. The next layer in the receiver can then determine how to process the erroneous packet.

The control circuit then controls the input/output circuitry in the step 42 to receive the next transmitted packet M.

A performance comparison between the diversity automatic repeat request scheme of the present invention and the basic automatic repeat request scheme described in the introduction hereinabove is shown in Figures 3 and 4.

Figure 3(a) is a plot of retransmissions against signal-to-noise ratio, Figure 3(b) is a plot of delay (in seconds) against signal-to-noise ratio, and Figure 3(c) is a plot of throughput (in bits per second) against signal to noise ratio. In Figures 3(a) to 3(c) the lines 200 represent the performance of the diversity ARQ scheme of the present invention, the lines 202 represent the prior art ARQ combiner performance, and the lines 204 represent the basic ARQ performance.

15 It can be seen from the simulation results of Figure 3 that the diversity-ARQ mechanism of the present invention out-performs the basic ARQ mechanism throughout. In particular at low signal-to-noise ratios the throughput is almost three times higher with the diversity ARQ than with the basic ARQ.

Figure 4 shows a comparison of the bit error rates (BERs) obtained after two and three block transmissions per RLC/MAC block. Line 208 illustrates performance for two block transmissions, and line 206 illustrates performance for three block transmissions. As can be seen from Figure 4 after three retransmissions (represented by line 206), at a signal-to-noise ratio greater than 6dB the average bit error rate goes almost to zero. This is obtained at an increase in the block transfer delay. In all the above simulations coding scheme 1 (CS-1 of GPRS) was used.

Claims

- 1) A method of recovering a received packet comprising the steps of:
 - a) generating a soft value for each bit of the received packet;
 - b) storing the soft values of the received packet;
 - 5 c) performing an error check on the received packet; and
 - d) responsive to detection of an error:
 - i) receiving a retransmission of the packet;
 - ii) generating a soft value for each bit of the retransmitted packet;
 - 10 iii) combining each generated soft value with the respective last stored soft values;
 - iv) storing the combined soft values;
 - v) performing an error check based on the thus combined soft values; and
 - vi) responsive to detection of an error repeating steps i) to v).
- 15 2) The method of claim 1 wherein the step of combining each soft output value of the retransmitted packet with the respective stored soft output value comprises adding the respective soft values.
- 3) The method of claim 1 or claim 2 further comprising the step of determining a hard value from the soft values of the received packet.
- 20 4) The method of claim 3 wherein the error check of step c) is performed on said hard value.
- 5) The method of any preceding claim further comprising the step of determining a hard value from the combined soft values.
- 6) The method of claim 5 wherein the error check of step v) is performed on
- 25 said hard value.
- 7) The method of any one of claims 1 to 4 wherein if no error is detected in step c) the hard value forms an output.

- 8) The method of any one of claims 1 to 6 wherein if no error is detected in step v) the hard value forms an output.
- 9) The method of any preceding claim further comprising the step, prior to the step a) or i), of equalising the received packet.
- 5 10) The method of any preceding claim, wherein the error check comprises a cyclic redundancy code check.
- 11) The method of any preceding claim wherein in step vi), steps i) to v) are repeated a predetermined number of times.
- 12) The method of any preceding claim wherein in step vi), steps i) to v) are
10 repeated for the maximum number of retransmissions allowed by the system, or for the maximum delay per packet.
- 13) The method of operating a receiver of a mobile communications system according to any one of claims 1 to 13.
- 14) A receiver comprising:
- 15 a) input circuitry for receiving a transmitted packet;
- b) generating circuitry, connected to the input circuitry, for generating a soft value for each bit of the received packet;
- c) storage circuitry for storing the thus generated soft values;
- d) error checking circuitry for performing an error check on the received
20 packet; and
- e) combining circuitry, wherein responsive to detection of an error:
- i) the input circuitry receives a retransmission of the packet;
- ii) the generating circuitry generates a soft value for each bit of the retransmitted packet;
- 25 iii) the combining circuitry combines each generated soft value with the respective stored soft values;

16

iv) the storage circuitry stores combined soft values in place of the stored soft values;

v) the error checking circuitry performs an error check based on the thus combined soft values,

5 vi) wherein i) to v) are repeated responsive to detection of an error in v).

15) A mobile communications system including the receiver of claim 14.

ABSTRACT

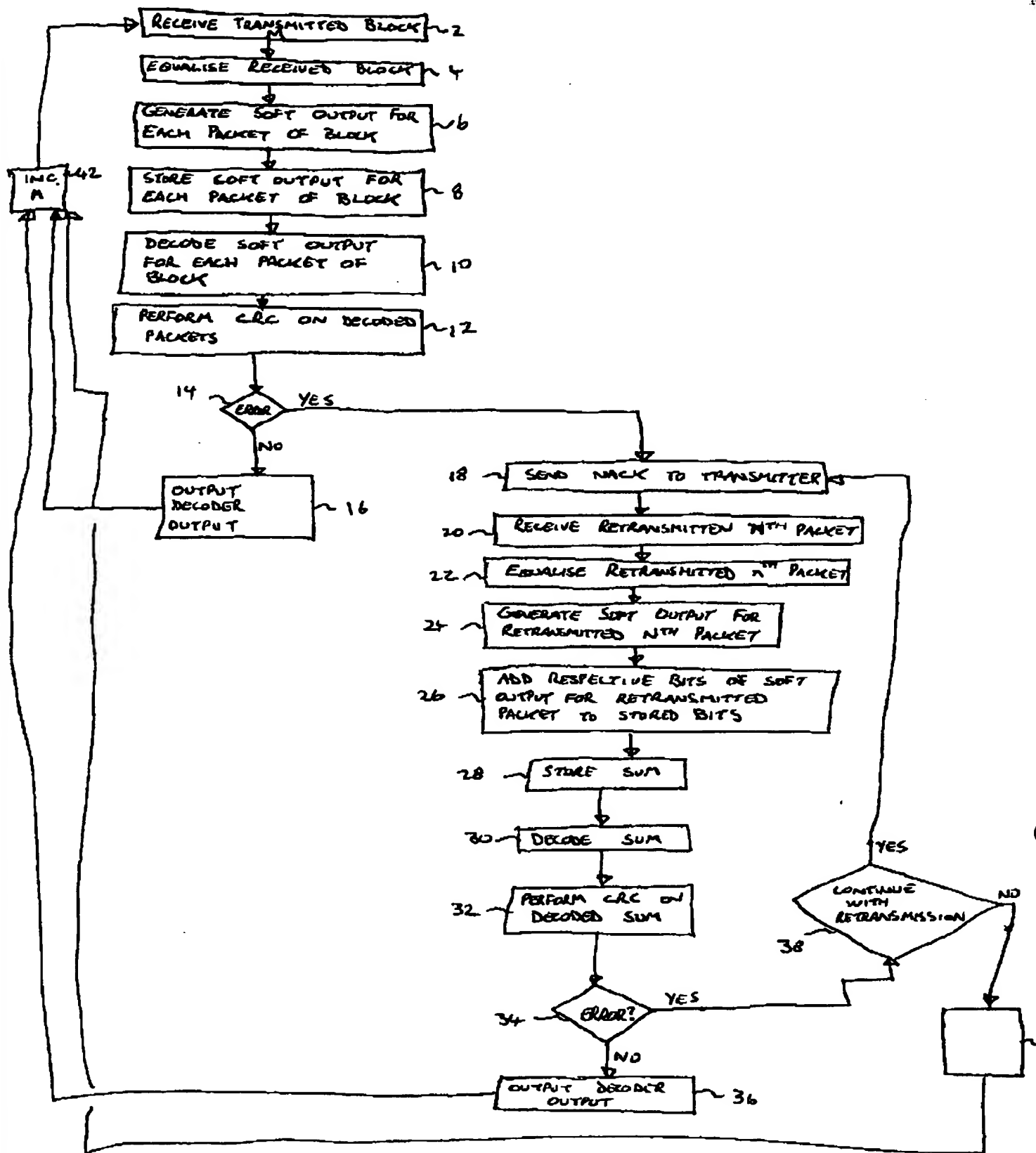
There is disclosed a method of recovering a received packet comprising the steps of: generating a soft value for each bit of the received packet; storing the soft values of the received packet; performing an error check on the received packet; and responsive to detection of an error:

- i) receiving a retransmission of the packet;
- ii) generating a soft value for each bit of the retransmitted packet;
- iii) combining each generated soft value with the respective last stored soft values;
- 10 iv) storing the combined soft values;
- v) performing an error check based on the thus combined soft values; and
- vi) responsive to detection of an error repeating steps i) to v).

Circuitry for implementing such a method in a receiver is also disclosed.

15 [Figure 1]

114

FIGURE 1

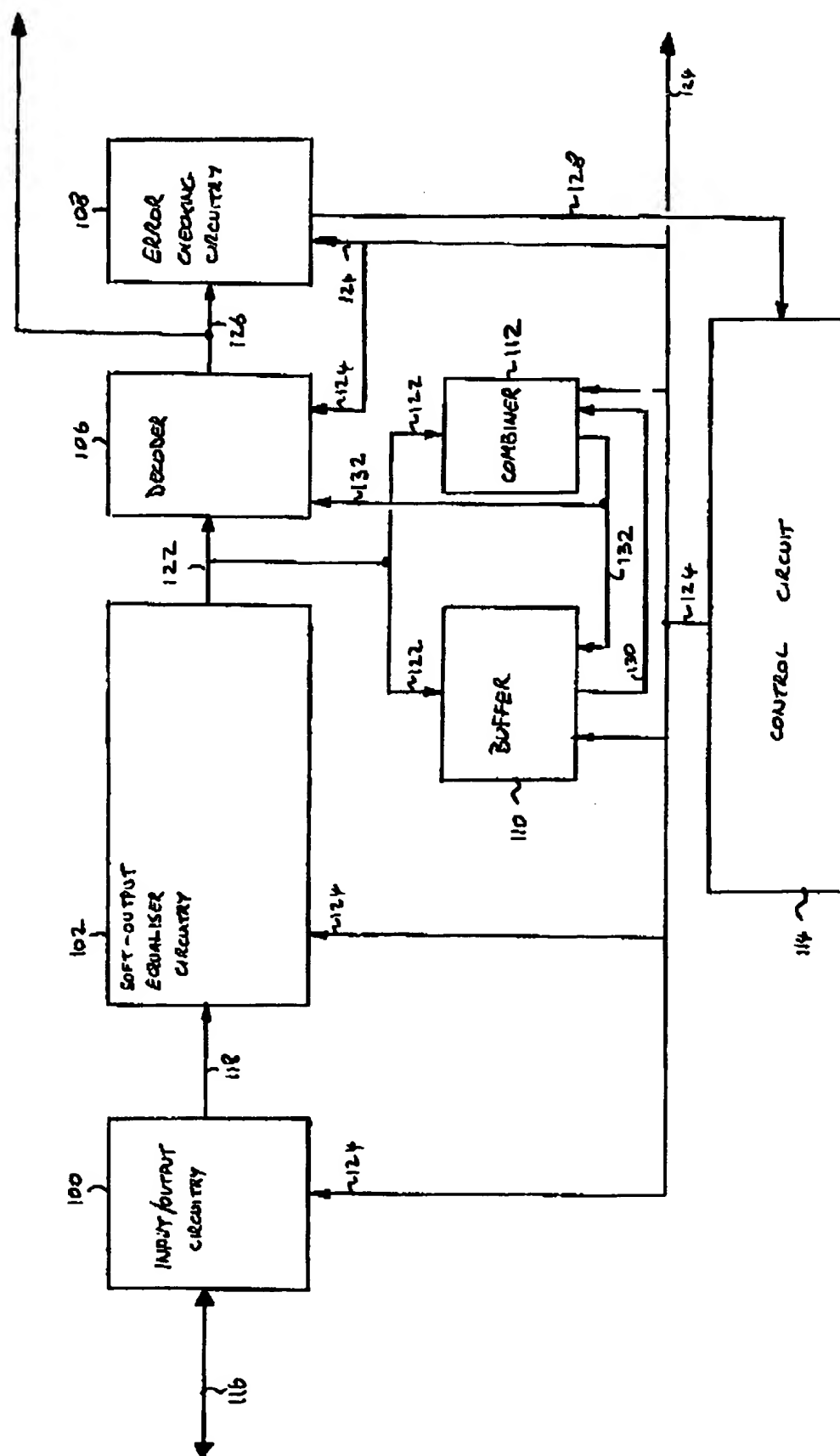


FIGURE 2

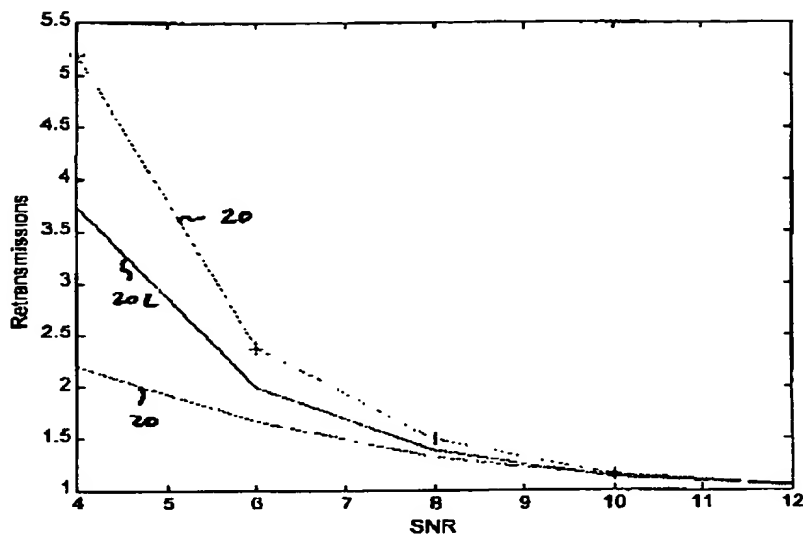


Figure 3(a)

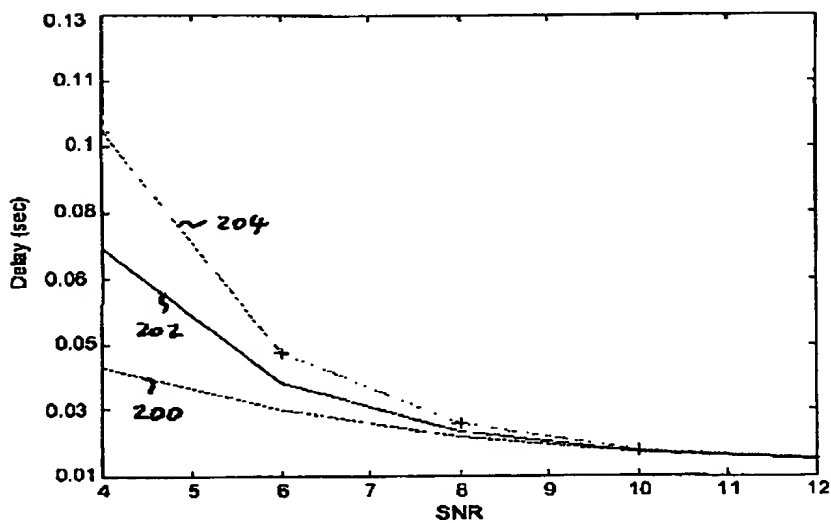


Figure 3(b)

4/4

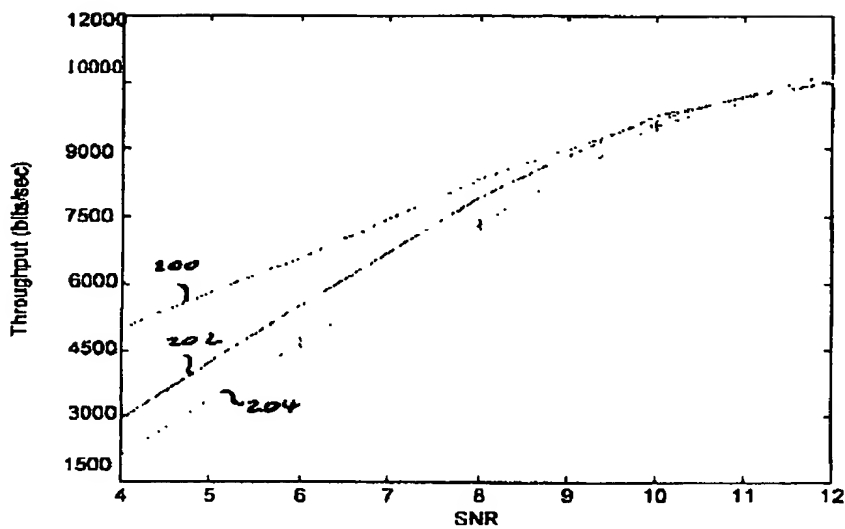


Figure 3(c)

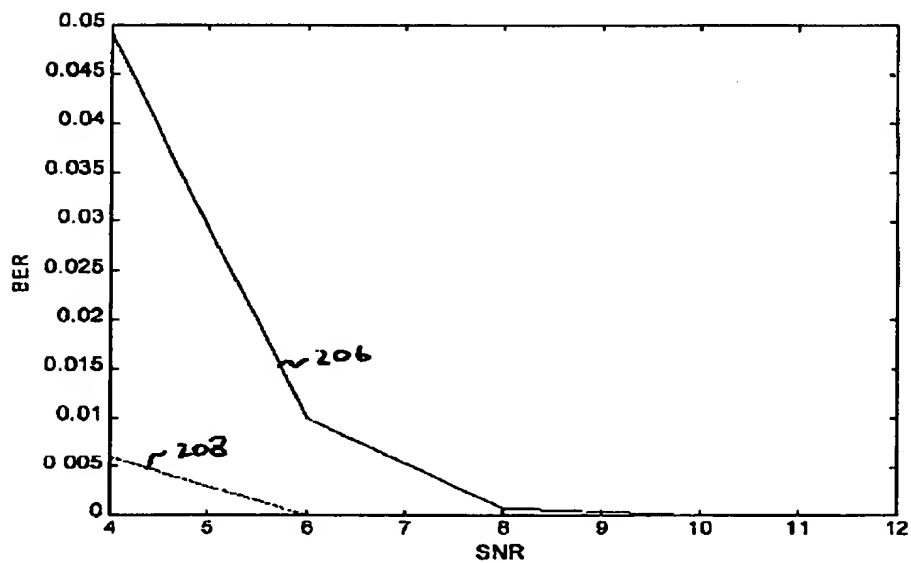


Figure 4

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